THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KEITH BALMER

Appeal No. 96-4184 Application No. 08/159,346¹

ON BRIEF

Before THOMAS, HAIRSTON, and LALL, <u>Administrative Patent</u> <u>Judges</u>.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1, 2, 4 through 11, 13 through 34, 36 through 42, 44 through 76 and 78 through 113. In an Amendment After Final (paper number 7), claims 1, 10, 34, 41, 42, 49, 68 and 76 were amended. As

¹ Application for patent filed November 30, 1993.

a result of the amendment, the examiner withdrew the indefiniteness rejection of claims 1, 2, 4 through 11, 13 through 34, 36 through 42, 44 through 64, 68 through 72, 76, 78 through 80, 96 through 107, 109, 110, 112 and 113 (paper number 8). After considering appellant's arguments (Brief, pages 5 through 23), the examiner allowed claims 1, 2, 4 through 11, 13 through 34, 36 through 42, 44 through 64, 73 through 76, 78 through 107 and 111 through 113, and objected to claims 68 through 72, 109 and 110 as being dependent upon a rejected base claim, but indicated that they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Accordingly, claims 65 through 67 and 108 remain before us on appeal.

The disclosed invention relates to the rotation of bits in a plurality of data registers connected in a loop. The plurality of data registers are in a data processing apparatus.

Claim 65 is the only independent claim on appeal, and it reads as follows:

65. A data processing apparatus comprising:

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a data processor bus;

a plurality of N data registers connected to said data processor bus, said N data registers connected together in a loop with a most significant bit of one data register connected to a least significant bit of a sequential data register, a most significant bit of a last sequential data register connected to a least significant bit of a first sequential data register; and

a register selection circuit connected to said N data registers, said register selection circuit

selecting a specified data register for read access via said data processor bus in a normal register read mode,

selecting a specified data register for write access via said data processor bus in a normal register write mode, and

rotating the bits in each data register within said loop in a register rotation mode.

The references relied on by the examiner are:

Meltzer	4,368,513	Jan. 11,
1983		
Kloker	4,744,043	May 10,
1988		
Cornaby	5,410,722	Apr. 25,
1995		
		(filed Jan. 21,
1993)		

Claims 65 through 67 stand rejected under 35 U.S.C. § 103 as being unpatentable over Cornaby in view of Meltzer.

Claim 108 stands rejected under 35 U.S.C. § 103 as being unpatentable over Cornaby in view of Meltzer and Kloker.

Reference is made to the briefs and the answers for the respective positions of the appellant and the examiner.

OPINION

The obviousness rejections of claims 65 through 67 and 108 are reversed.

According to the examiner (Answer, page 4), Cornaby discloses "registers connected in a loop (col. 6, line 61, et seq.)," but does not "specifically disclose rotating the bits in each data register within the loop."

The examiner is of the belief (Answer, page 4) that

Meltzer discloses data registers "connected in a loop (col. 8,

line 42, et seq.) and the bits of the data registers being

rotated within the loop (col. 8, line 54, et seq.)."

Based upon the teachings of Meltzer, the examiner concludes (Answer, page 4) that "[i]t would have been obvious to one of ordinary skill in the art at the time of Appellant's invention to include Meltzer's teaching of data rotation into the Cornaby system, because such would increase the versatility of the Cornaby system by allowing for shifting of data amongst data registers."

Appellant argues (Supplemental Reply Brief, page 3) that:

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In claims . . . 65, 66 . . . the plurality of data registers are connected in one loop and the normal read and write operations include plural bits within the single loop. Meltzer states at column 8, lines 54 to 59:

"The shift register loops on the pages of the file are rotated synchronously, in the direction shown by the arrows, both with respect to loops within a page an [sic, and] with respect to loops in different pages so that all bits constituting Bytes K in Pages 1-N appear at read/write ports 21, 22, 23, . . . and 2N at the same time."

This portion of Meltzer clearly teaches plural loops. In addition, this portion of Meltzer further teaches that the read/write operations occur simultaneously in all the loops. Thus Meltzer cannot write to or read from plural bits of data within a single loop as required by the recitations of claims . . . 65, 66

Meltzer clearly states (column 8, lines 39 through 46) that each of the Loops 1 through M is configured as a single shift register loop (Figure 1), with each loop having 4,096 bit storage positions (i.e., Bit 0 to Bit 4,095). We agree with appellant that Meltzer discloses "plural loops" of shift registers, and not "a loop" of registers as claimed. The plurality of shift register loops in Meltzer are connected in parallel for reading or writing of an M-bit byte, and all of

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the shift register loops are "rotated synchronously" (column 5, lines 28 through 30; column 8, lines 51 through 59).

In summary, the obviousness rejection of claims 65 through 67 is reversed because Meltzer's parallel-connected shift register loops are completely different from the claimed plurality of serially-connected data registers in "a" loop.

The obviousness rejection of claim 108 is reversed because the teachings of Kloker cannot cure the noted shortcomings in the teachings of Cornaby and Meltzer.

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DECISION

The decision of the examiner rejecting claims 65 through 67 and 108 under 35 U.S.C. § 103 is reversed.

REVERSED

JAMES D. THOMAS Administrative Patent	Judge)
)
KENNETH W. HAIRSTON)) BOARD OF PATENT) APPEALS
Administrative Patent	Judge) AND) INTERFERENCES
)
)
PARSHOTAM S. LALL Administrative Patent	Judge)

lp

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DECISION: <u>REVERSED</u> Send Reference(s): Yes No

or Translation (s)

Panel Change: Yes No

Index Sheet-2901 Rejection(s): _____

Prepared: June 8, 2000

Draft Final

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OB/HD GAU

PALM / ACTS 2 / BOOK DISK (FOIA) / REPORT